In the Claims:

1. (Original) Charge-trapping memory device comprising:

a semiconductor body or substrate with at least one memory cell arranged in said semiconductor body or substrate;

source and drain regions formed by doped regions in said semiconductor body or substrate and limited by junctions;

a gate dielectric on a surface of said semiconductor body or substrate between said source and drain regions and having a layer thickness;

a gate electrode on said gate dielectric; and

a charge-trapping layer formed within said gate dielectric,

the charge-trapping layer comprising two strips which are each located between an upper boundary of said junctions and said gate-electrode and which are enclosed by said gate dielectric,

said strips being formed of a material with higher relative permittivity than the gate dielectric, and

said strips having a layer thickness which is provided relative to said layer thickness of said gate dielectric in an area between said strips and a total layer thickness of said gate dielectric in an area of said strips in such a manner that a positive voltage applied to said gate electrode and provided for inducing a Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer generates an electric field strength in said area of said strips, which is larger or equal to an electric field strength in said area between said strips during a process of erasure of said memory cell.

2. (Currently Amended) Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is silicon nitride; and

[[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.3 and 0.7.

3. (Currently Amended) Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is Al_2O_3; and [[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.25 and 0.6.

4. (Currently Amended) Charge-trapping memory device according to claim 1, in which said gate dielectric is silicon dioxide and said charge-trapping layer is HfO_2; and [[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.2 and 0.5.

5. (Original) Charge-trapping memory device according to claim 1, in which said total layer thickness of said gate dielectric in said area of said strips is larger than said layer thickness of said gate dielectric in said area between said strips.

6. (Currently Amended) Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is silicon nitride; and

[[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.3 and 0.7.

7. (Currently Amended) Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is AJ_2O_3; and [[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.25 and 0.6.

8. (Currently Amended) Charge-trapping memory device according to claim 5, in which said gate dielectric is silicon dioxide and said charge-trapping layer is HfO_2; and [[the]] a ratio of said layer thickness of said charge-trapping layer and said layer thickness of said gate dielectric in said area between said strips is between 0.2 and 0.5.

9. (Original) A memory device comprising:

a semiconductor body or substrate with at least one memory cell arranged in said semiconductor body or substrate;

source and drain regions formed by doped regions in said semiconductor body or substrate and limited by junctions;

a gate dielectric on a surface of said semiconductor body or substrate between said source and drain regions and having a layer thickness;

a gate electrode on said gate dielectric; and

a charge-trapping layer formed within said gate dielectric,

the charge-trapping layer comprising two strips which are each located between an upper boundary of said junctions and said gate-electrode and which are enclosed by said gate dielectric,

said strips being formed of a material with higher relative permittivity than the gate

dielectric, and

said strips having a layer thickness which is provided relative to said layer thickness of said gate dielectric in an area between said strips and a total layer thickness of said gate dielectric in an area of said strips in such a manner that a positive voltage applied to said gate electrode and provided for inducing a Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer generates an electric field strength in said area of said strips, which is larger or equal to an electric field strength in said area between said strips during a process of erasure of said memory cell;

wherein said memory cell is erased by applying a positive voltage to said gate electrode to induce Fowler-Nordheim-tunnelling of electrons into said charge-trapping layer;

said memory cell is programmed at one of said strips of said charge-trapping layer individually by hot hole injection effected by a negative voltage applied to said gate electrode and a positive voltage applied to one of said source and drain regions adjacent to said strip; and

said memory cell is read by applying a voltage between said source and drain regions of said memory cell, which is reverse to a voltage applied for programming.

10. (Original) The memory device according to claim 9, whereby,

in an array of memory cells comprising:

at least a first memory cell and a second memory cell adjacent to said first memory cell; and

a continuous doped region comprising as integral parts thereof a first one of said source and drain regions of said first memory cell and a first one of said source and drain regions of said second memory cell;

said first memory cell is programmed at one of said strips of said first memory cell adjacent to said first one of said source and drain regions of said first memory cell, by applying a positive inhibit voltage to a second one of said source and drain regions of said second memory cell.

11-14. (Canceled)